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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,448	12/10/2001	Robert Thomas Bailis	RPS920010128US1	5281

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	**PAPER NUMBER**
2133	5

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,448	BAILIS ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on April 15, 2002 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

The formal drawings were received on April 15, 2002. These drawings are acceptable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salem et al. U.S. Patent No. 5,844,917 in view of Laberge et al. U.S. Patent No. 6,012,148.

As per claim 1, Salem et al teach an adapter card with an application specific integrated circuit (ASIC) a field programmable gate array (FPGA), and program logic device (PLD), i.e. gate array logic. The PLD communicates with the system over I/O bus. The system can also communicate directly with FPGA via I/O bus. Test controls are sent from the FPGA to the ASIC. Data is scanned into the ASIC, and scanned out of the ASIC. The PLD and FPGA each contain one or more programmable options select (POS) registers. The FPGA also contains a scan state machine and a self-test state machine. (FIG. 2, column 2 lines 39-52) Not explicitly disclosed is that the contents of this test cards are located on a single ASIC.

However, in an analogous art, Laberge et al. teach that as today's computer systems are continually enhanced with respect to speed and computing power, the

intricate nature and complexity often increases in parallel. To maintain a high degree of reliability in such systems, error processing is used to locate, report, and act on system faults and faults within particular components within the system. Scan testing is often used for custom VLSI chips and ASICs, because the internal signals simply are not accessible. Scan methods considers any digital circuit to be a collection of registers or flip-flops interconnected by combinatorial logic where test patterns are shifted into a large shift register organized from the storage elements of the circuit (column 1 lines 11-33). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the system of Salem et al. on a single ASIC. This would have been obvious as suggested by Laberge et al. (column 1 lines 13-19). To maintain a high degree of reliability in such systems, error processing is used to locate, report, and act on system faults and faults within particular components within the system. Error processing is important during the real-time execution of the computer system, but is also important during system test.

As per claims 2-4, Salem et al. teach the use of multiplexers as a connection for signals through programmable devices used in order to test the logic (column 2 lines 43-46, column 3 lines 5-8, and 25-34).

As per claims 5, 6, 12, and 14 based on test controls from the FPGA (one example of reconfigurable logic) to ASIC, test data is provided to the ASIC. The test data is then operated on within the ASIC to exercise the one or more logic functions of the ASIC. Finally, a determination is made as to whether the output data from the ASIC

contains any errors based on the software (figure 10, column 4 line 62 through column 5 line 7).

As per claim 7, Laberge et al. teach an error detection and recovery apparatus for monitoring, and recovering from, errors in a system having one or more logic units. Abstract

As per claims 8, 9, 13, and 15, Laberge et al. teach that a microsequencer can recover from error. The microsequencer receives the particular error signal via bus, which provides the error A, error B through error n signals from the error A field. The ability for the microsequencer to read the error register allows the microsequencer to perform error analysis, as it therefore knows the particular error that occurred. The microsequencer includes recovery routines which can be stored at the microsequencer itself, or alternatively in a separate memory device. These microcode recovery routines are prepared in advance and written to properly recover from an error presented to the microsequencer. A microcode recovery routine can be triggered in response to a particular error. Using recovery code allows a test to continue to run despite the fact that known hardware problem exists. Furthermore, this also allows known hardware problems to be corrected without having to correct defective hardware in a custom chip (column 7 lines 28-61 Figure 2).

As per claims 10, 11, 18 and 19, Laberge et al. teach that a support controller may itself monitor a particular unit, or may act on a reported error originating from a particular unit or "watchdog" hardware/software component, which monitors for specific faults and reports them to the support controller. (Column 1 lines 45-49)

As per claims 16 and 17, Laberge et al. teach I an error detection and recovery circuit for monitoring for system errors. The system may include one or more individual logic units that together makes up the complete system. An error detection mechanism is provided to detect the errors in any of the logic units, and to provide error signals to indicate which of the logic units had an error and what error occurred. A first error recovery mechanism receives the error signals, and can perform a system-level recovery based on the particular error that occurred. A second error recovery mechanism also receives the error signals, and can perform a unit-level recovery. The error history is recorded from the bus history analyzer. (Column 3 lines 4-49)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Boundary Scan Access of Built-in Self-test for Field Programmable Gate Arrays" by Gibson et al. Tenth Annual IEEE International Proceedings ASIC Conference and Exhibit Publication Date: 7-10 Sept. 1997, pages 57 – 61, Inspec Accession Number: 5774208

This paper teaches issues associated with system level access of Built-In Self-Test (BIST) for Field Programmable Gate Arrays (FPGAs) via the Boundary Scan Interface. In addition, we describe the design of an Application Specific Integrated Circuit (ASIC) which serves as an interface between a PC parallel port and the Test

Access Port (TAP) of one or more FPGAs to reprogram the FPGA(s) and administer BIST during off-line testing. We also include a brief description of the FPGA BIST architecture and operation

"pFSB Technology Enables Field Programmability in an ASIC Environment" by Coli et al. in Digest of Papers Compcon Spring '93, Publication Date: 22-26 Feb. 1993, pages: 385 - 389 Inspec Accession Number: 4750288

This paper teaches pFSB (programmable functional system blocks) technology and cells, a field-programmable capability based on ViaLink antifuse technology that can be embedded in an ASIC chip. Fully compatible with existing high-speed ASIC processing, library cells, compilers, and design tools, pFSB cells give the user an extension of traditional ASIC technology that provides for additional value in both ASIC- and ASSP (application specific signal processor) based systems. Chips using pFSB structures, as memory, logic, or customized elements, give the designer the ability to make last-minute decisions in product design, as well as allowing the security of designs to be easily implemented. The availability of comprehensive testing and programming hardware and software results in a user environment for chips using pFSB cells that is both friendly and easily implemented. The authors present a description of the ViaLink programming element, a description of pFSB cells and how they are used, and a summary of design methodology, testing, and programming considerations

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

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